Front-end electronics and hit position reconstruction methods for the J-PET scanner

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J-PET TOMOGRAPHY SCANNER

The J-PET collaboration is developing a prototype PET based on plastic scintillators, which allows for single-bed-imaging of the whole human body [1-5]. This novel approach exploits the excellent time properties of the plastic scintillators, which permit very precise time measurements of the signals allowing for the effective usage of the Time-of-Flight (TOF) technique.

CHANGE OF THE PARADIGM

Crystal → Plastic
Energy → Time
High granularity → Low granularity
High efficiency → Low efficiency
Low acceptance → High acceptance
Analog electronics → Digital electronics
Triggering → No master trigger

AFOV = 50 cm
(axial field of view)

CRT = 300 ps
(concidence resolving time)

PRECISE HIT POSITION RECONSTRUCTION

This multi-level threshold technique is well suited for the application of reconstruction methods of the gamma hit position in the scintillator, which results in the improvement of the TOF resolution. The compressive sensing technique allows for the recovery of the full signal shape and amplitude based on the samples registered in the PMTs, which can be used to improve the precision of the hit reconstruction [8-9]. Other methods are based on the comparison of detected signals with results stored in a library of synchronized model signals registered for a set of well-defined positions of scintillation points [5,7].

FRONT-END ELECTRONICS (FEE)

A novel ultrafast front-end electronics allowing for sampling in the voltage domain of the signals with a duration of few nanosecond was developed [6]. The FEE solution is a purely digital implementation, based solely on a FPGA (Field Programmable Gate Array) device and few satellite discrete electronic components.

The input signals are amplified and split into four paths, each having an individual threshold level. The design includes only DAC chips (LTC2620) for threshold settings and passive splitters connected to the FPGA. Low Voltage Differential Signalling (LVDS) buffers. Time to digital conversion is realized in the FPGA and it is based on low-delay carry-chains usually used as part of adders.

The solution allows to probe the signal in the voltage domain with an accuracy below 20 ps (σ). An additional advantage of the FPGA solution is a very low cost. At present, in the prototype phase, one sample together with digitization costs only about 10 Euro.

REFERENCES